

A cross-sectional view of a semiconductor device. A central channel region 108 is flanked by two side regions 104 and 106. The device is built on a substrate 100. A gate stack 103 is located on top of the channel and side regions. The gate stack consists of a gate dielectric 109 and a gate electrode 110. The side regions 104 and 106 are covered by a layer 105. The channel region 108 is covered by a layer 107. The substrate 100 has a top surface 101 and a bottom surface 102. The channel region 108 has a width 111 and a height 112. The side regions 104 and 106 have a width 113 and a height 114. The gate stack 103 has a thickness 115. The gate dielectric 109 has a thickness 116. The gate electrode 110 has a thickness 117. The layer 105 has a thickness 118. The layer 107 has a thickness 119. The substrate 100 has a thickness 120.

FIG 3a

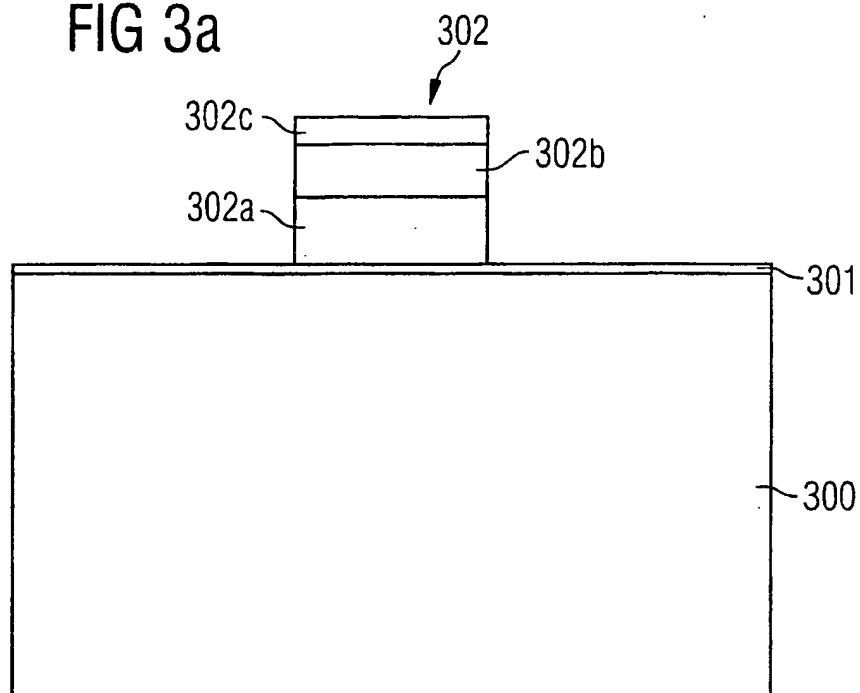


FIG 3b

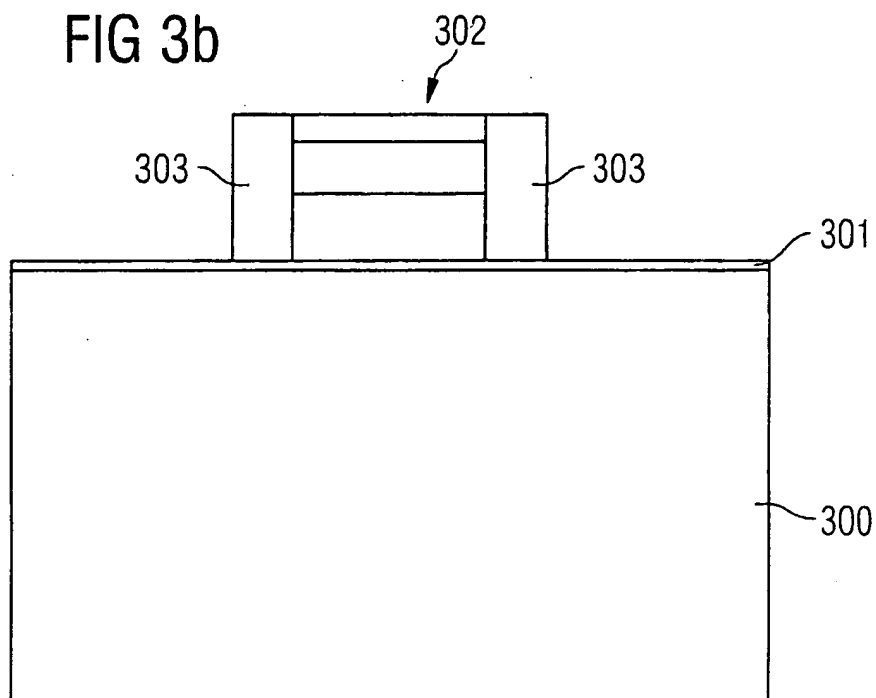


FIG 3c

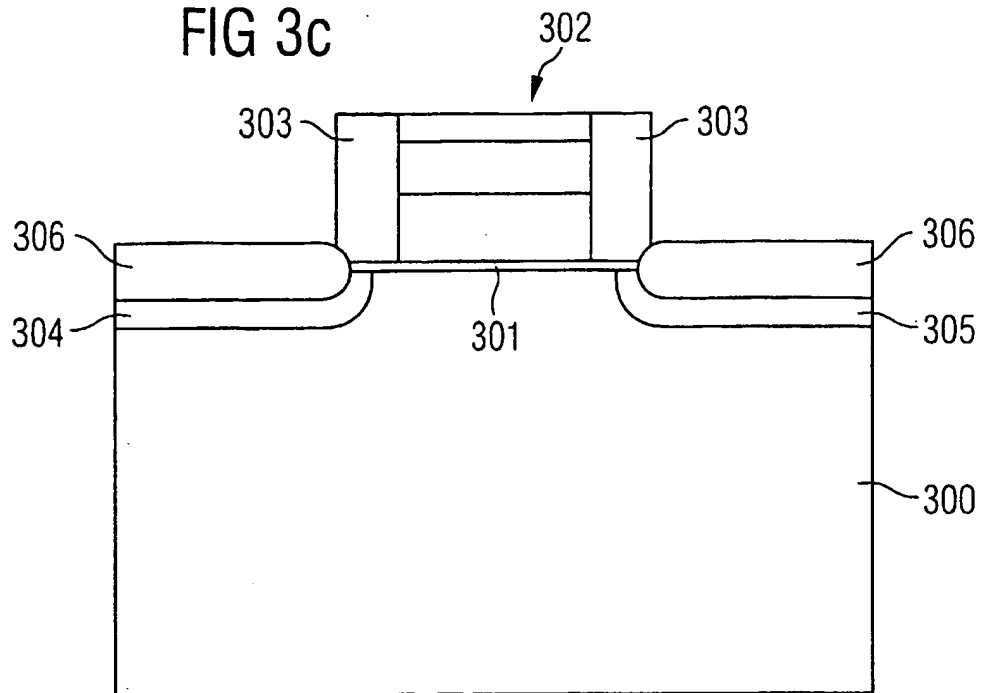


FIG 3d

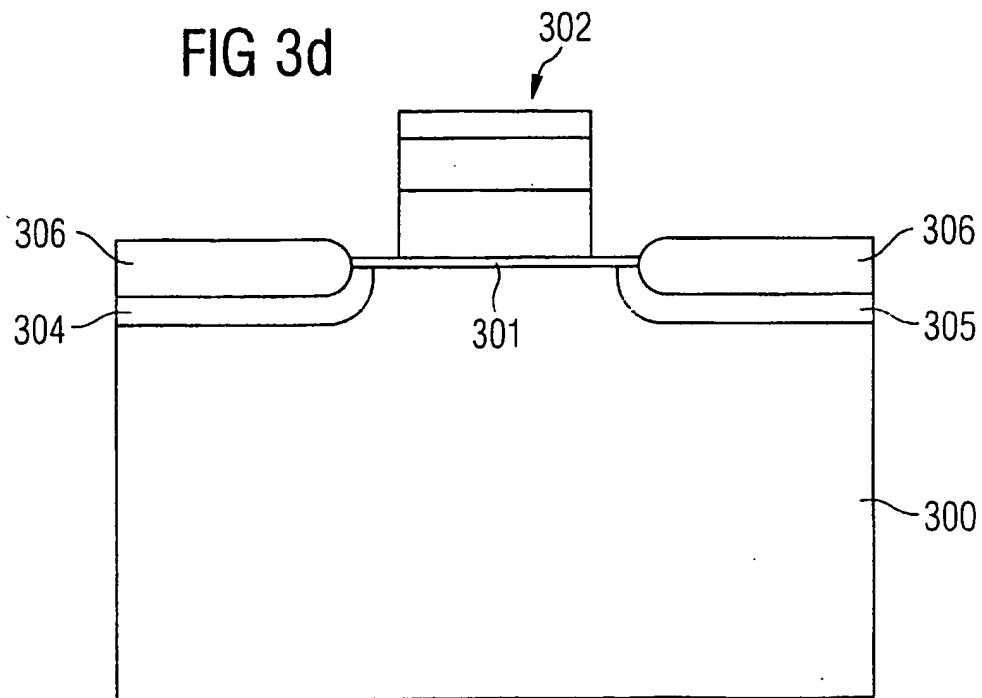


FIG 3e

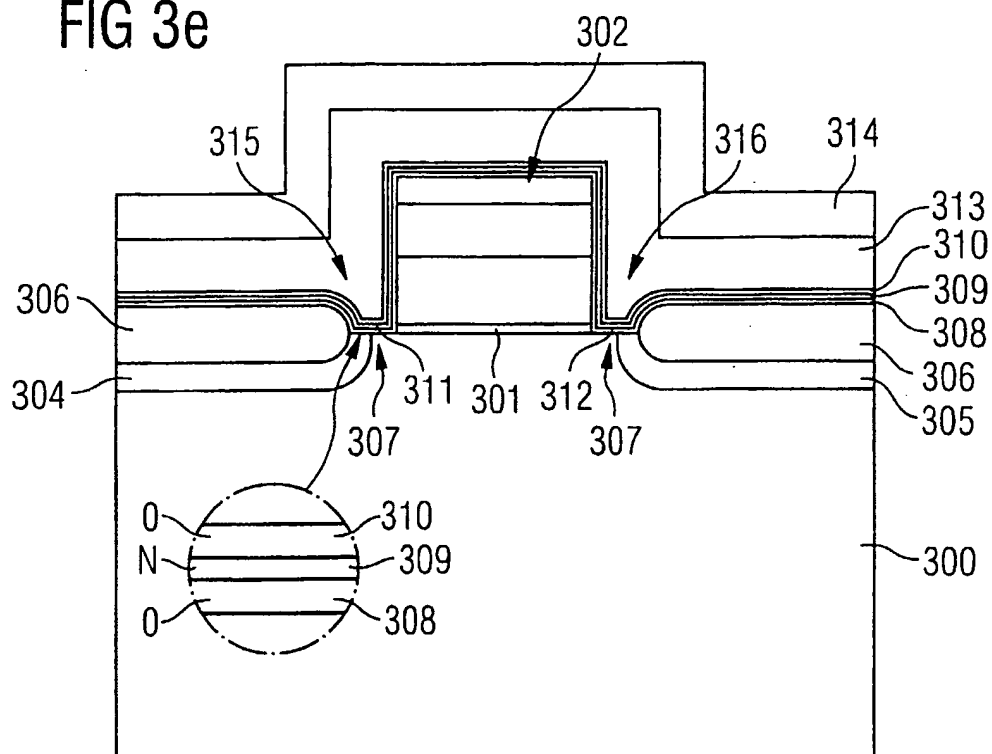


FIG 3f

